March 14, 2005

UNITED STATES PATENT FINAL OFFICE ACTION REPLY

FOR

(TITLE):

SYSTEM AND METHOD FOR INTEGRATING A DIGITAL CORE WITH A SWITCH MODE POWER SUPPLY

APPLICANT:

ANDREW R. GIZARA

APPLICATION NUMBER:

10/604,573

FILING DATE:

07/31/2003

EXAMINER:

SHAWN RILEY

ART UNIT:

2838

PREPARED BY:

Andrew R. Gizara
24471 Corta Cresta Drive
Lake Forest, California 92630-3914
(949) 457-0751

4. (Previously Presented) An integrated circuit package comprising:

Application Number: 10/604,573 Examiner: Shawn Riley Art Unit: 2838 March 14, 2005

REPLY TO DETAILED ACTION

Specification

The final page of this Office Action Reply includes the currently amended Abstract of the disclosure to replace in its entirety the immediate prior Abstract. The currently amended abstract has one sentence amended from the immediate prior Abstract, to comply with the formal requirement to remove the purported merits therein. The prior amended sentence that contained the phrase "highest efficiency" has been rewritten as follows: "Within the integrated circuit package including this semiconductor die also exists a switch mode DC-to-DC voltage converter, preferably a synchronous step-down regulator powering the entire integrated circuit from one supply voltage."

Claim Objections

Since the examiner's final action indicates no objections to the allowable claims, the applicant understands the prior amendments comply with all formal requirements and no further traversal is necessary for these claims.

Claim Rejections

The applicant hereby requests reconsideration of claim 1 and claim 14 as currently amended to include within the clause of "output voltage fixing circuit", the further limitation of "output voltage fixing circuit comprising digital open-loop means requiring no feed-forward loop and no feedback loop."